

91 sides from a phase-locked loop circuit, respectively, the first equalization circuit on the upstream side including a transversal filter to minimize an equalization error caused by the first equalization circuit and to stabilize the operation of the phase-locked loop circuit. Another signal-processing circuit including an analog-to-digital converter and a digital phase-locked loop circuit for receiving the output from the analog-to-digital converter and a recording and playback apparatus using the output are also provided, wherein the output from the analog-to-digital converter is input as the digital signal in the digital phase-locked loop circuit to fetch a detection point voltage and to stabilize the phase-locked loop circuit without an analog circuit.--

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IN THE CLAIMS

Please amend claims 1-31 by rewriting same to read as follows:

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92 --1. (Amended) A signal-processing circuit, comprising:  
 a phase-locked loop circuit for receiving playback data resulting from analog-to-digital conversion of a playback signal from an equalization circuit,  
 wherein said first equalization circuit is composed of a transversal filter.

--2. (Amended) The signal-processing circuit according to claim 1, wherein said equalization circuit includes means

for performing adaptive equalization.

--3. (Amended) The signal-processing circuit according to claim 1, wherein said equalization circuit comprises a first equalization circuit and further comprising a second equalization circuit provided on a downstream side from said phase-locked loop circuit, wherein

a sampling frequency of said first equalization circuit is made approximately equal to a channel clock frequency;

a subsequent transfer characteristic of said first equalization circuit is made equal to a product of a present transfer characteristic of said first equalization circuit and a present transfer characteristic of said second equalization circuit; and

a subsequent transfer characteristic of said second equalization circuit is flattened.

--4. (Amended) The signal-processing circuit according to claim 3, wherein said transversal filter is used for each of said first equalization circuit and said second equalization circuit to obtain said subsequent transfer characteristic of said first equalization circuit by setting a subsequent tap coefficient of said first equalization circuit to a result of a convolutional integration of a present tap coefficient of said first equalization circuit and a present tap coefficient of said second equalization circuit.

--5. (Amended) The signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on a downstream side from said phase-locked loop circuit,

wherein said equalization circuit is subjected to adaptive equalization by applying tap-coefficient-updating information output by said adaptive equalization circuit to a tap coefficient of said first equalization circuit in accordance with:

subsequent k-th tap coefficient = present k-th tap coefficient + k-th tap-coefficient-updating information.

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--6. (Amended) The signal-processing circuit according to claim 1, wherein said equalization circuit comprises a first equalization circuit and further comprising a second equalization circuit provided on a downstream side from said phase-locked loop circuit, wherein

a sampling frequency of said first equalization circuit is set at a value higher than a channel clock frequency;

a subsequent transfer characteristic of said first equalization circuit is divided into a portion in a first frequency band being within a frequency band of said second equalization circuit and a portion in a second frequency band being outside of said frequency band of said second equalization circuit;

said portion of said subsequent transfer characteristic of said first equalization circuit in said first frequency

band is taken as a product of a portion of said present time transfer characteristic of said first equalization circuit in said first frequency band and said present transfer characteristic of said second equalization circuit, and said portion of said subsequent transfer characteristic of said first equalization circuit in said second frequency band is set to zero; and

said subsequent transfer characteristic of said second equalization circuit is flattened.

az --7. (Amended) The signal-processing circuit according to claim 6, wherein said transversal filter is used for each of said first and said second equalization circuits to determine a subsequent tap coefficient of said first equalization circuit by:

obtaining a tap coefficient A of said first equalization circuit by subjecting a present tap coefficient of said first equalization circuit to  $f_c/S_1$  thinning, where  $S_1$  denotes a sampling frequency of said first equalization circuit and  $f_c$  denotes a channel clock frequency;

obtaining a convolution-integration result C in accordance with  $C = A * B$ , where  $*$  denotes a convolution-integration operator and B denotes a present tap coefficient of said second equalization circuit;

obtaining a tap coefficient D by subjecting said convolution-integration result C to  $S_1/f_c$ -times interpolation; and

taking said tap coefficient D as said subsequent tap coefficient of said first equalization circuit.

--8. (Amended) The signal-processing circuit according to claim 6, wherein said transversal filter is used for each of said first and second equalization circuits to determine a subsequent tap coefficient of said first equalization circuit by:

obtaining a tap coefficient B of said second equalization circuit by subjecting a present tap coefficient of said second equalization circuit to  $f_c/S_1$  thinning, where  $S_1$  denotes a sampling frequency of said first equalization circuit and  $f_c$  denotes a channel clock frequency;

obtaining a convolution-integration result C in accordance with  $C = A * B$ , where  $*$  denotes a convolution-integration operator and A denotes a present tap coefficient of said first equalization circuit; and

taking said convolution-integration result C as said subsequent tap coefficient of said first equalization circuit.

--9. (Amended) The signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on a downstream side from said phase-locked loop circuit,

wherein said equalization circuit is subjected to said adaptive equalization by:

making a sampling frequency  $S_1$  of said equalization

circuit higher than a channel clock frequency  $f_c$ ;

obtaining a tap coefficient A by subjecting a present tap coefficient of said first equalization circuit to  $f_c/S_1$  thinning;

calculating a subsequent value of said tap coefficient A in accordance with:

subsequent k-th value of tap coefficient A = present k-th value of tap coefficient A + k-th tap-coefficient-updating information;

obtaining a tap coefficient B by subjecting said subsequent value of said tap coefficient A to  $S_1/f_c$ -times interpolation; and

setting said tap coefficient B to a subsequent tap coefficient of said first equalization circuit.

--10. (Amended) A signal-processing circuit, comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal and for outputting said digital signal; and

a digital phase-locked loop circuit for receiving said digital signal from said analog-to-digital converter,

wherein said digital signal output by said analog-to-digital converter is supplied to said digital phase-locked loop circuit to fetch a detection-point voltage.

--11. (Amended) The signal-processing circuit according to claim 10, further comprising an equalization circuit

A2 provided between said analog-to-digital converter and said phase-locked loop circuit,

wherein said equalization circuit includes a digital transversal filter.

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--12. (Amended) The signal-processing circuit according to claim 11, further comprising an interpolation circuit provided between said equalization circuit and said digital phase-locked loop circuit,

wherein said interpolation circuit is adapted to interpolate separate pieces of sampling data with a period approximately equal to a channel-clock period.

A3 --13. (Amended) The signal-processing circuit according to claim 12, wherein a sampling frequency of said analog-to-digital converter is approximately equal to a channel-clock frequency.

--14. (Amended) The signal-processing circuit according to claim 12, wherein said interpolation circuit includes a transversal filter for said interpolation and an R-times interpolation circuit; and

data is thinned at intervals of R taps of said transversal filter for said interpolation.

--15. (Amended) The signal-processing circuit according to claim 14, wherein said R-times interpolation circuit is

composed of R pieces of a plurality of transversal filters disposed in parallel.

--16. (Amended) The signal-processing circuit according to claim 12, wherein said interpolation circuit includes a low-magnification interpolation circuit that includes a transversal filter and a Q-times linear interpolation circuit provided on a downstream side from said low-magnification interpolation circuit.

--17. (Amended) The signal-processing circuit according to claim 16, wherein said Q-times linear interpolation circuit is composed of Q pieces of a plurality of interpolation circuits disposed in parallel.

--18. (Amended) The signal-processing circuit according to claim 12, wherein said phase-locked loop circuit includes:

a data selector for receiving R X Q parallel trains of S X R X Q-times interpolation data from said interpolation circuit and selecting one of 0 and 1 piece of said data closest to a detection point from said parallel trains of data for  $S > 1$ ;

a detection point computing circuit for controlling said data selector; and

a circuit for reporting one of 0 said detection points and 1 said detection point.



--19. (Amended) The signal-processing circuit according to claim 12, wherein said phase-locked loop circuit includes:

a data selector for receiving  $R \times Q$  parallel trains of  $S \times R \times Q$ -times interpolation data from said interpolation circuit and selecting one of 0, 1, and 2 pieces of said data closest to detection points from said parallel data for  $S \leq 1$ ;

a detection point computing circuit for controlling said data selector; and

a circuit for reporting one of 0, 1, and 2 said detection points.

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--20. (Amended) The signal-processing circuit according to claim 12, wherein said phase-locked loop circuit includes:

a plurality of data selectors for receiving  $P \times R \times Q$  parallel trains of  $S \times R \times Q$ -times interpolation data from said interpolation circuit and for selecting a number of said data closest to a plurality of maximum detection points from said parallel data, a quantity of data selectors in said plurality of data selectors being equal to  $D_{max}$ ;

a plurality of detection point computing circuits for controlling one of said plurality of data selectors; and

a circuit for reporting a plurality of detection points.

--21. (Amended) The signal-processing circuit according to claim 11, wherein said phase-locked loop circuit includes:

thinning period correcting means for absorbing

frequency deviations while being updated in accordance with:

$$d = d \pm \Delta d,$$

wherein  $d$  denotes a thinning period and  $\Delta d$  denotes a thinning period correction quantity; and

a value of said thinning period correction quantity  $\Delta d$  given to said thinning period correcting means is changed in accordance with a response speed.

93 --22. (Amended) The signal-processing circuit according to claim 11, wherein a buffer memory in which data output by said phase-locked loop circuit is stored and from which data is read with a clock signal is provided on a downstream side from said phase-locked loop circuit.

--23. (Amended) The signal-processing circuit according to claim 22, wherein said buffer memory has two memory banks; and

for  $S \leq 1$  odd-numbered detection point data and even-numbered detection point data output by said phase-locked loop circuit are stored alternately into said two memory banks of said buffer memory.

--24. (Amended) The signal-processing circuit according to claim 22, wherein said buffer memory has a plurality of memory banks, a quantity of memory banks in said plurality of memory banks being equal to  $D_{max}$ , wherein  $D_{max}$  is a maximum

number of detection points simultaneously output by said phase locked loop circuit for receiving P X R X Q parallel trains of S X R X Q-times interpolation data Dmax is expressed by:  $D_{\max} = \text{Int} (P/S) + 1$ ; and

when a number of detection points reported by said phase locked loop circuit is D and D is one of less than and equal to Dmax detection point data output by said phase-locked loop circuit are stored in said buffer memory having said D banks.

93 --25. (Amended) The signal-processing circuit according to claim 22, wherein a frequency of said clock signal for reading data from said buffer memory is higher than a frequency of a channel clock signal.

--26. (Amended) The signal-processing circuit according to claim 25, wherein said buffer memory includes:

an empty-buffer detection circuit for outputting an empty-data signal to indicate that said buffer memory is empty,

wherein an operation of circuits provided at a back of said empty-buffer detection circuit is stopped based on said empty-data signal.

--27. (Amended) The signal-processing circuit according to claim 22, further comprising a voltage-controlled oscillator for generating said clock signal for reading said

data from said buffer memory.

--28. (Amended) The signal-processing circuit according to claim 27, wherein an oscillation frequency of said voltage-controlled oscillator is controlled to prevent an empty-data state and a data overflow in said buffer memory.

--29. (Amended) The signal-processing circuit according to claim 28, wherein said voltage-controlled oscillator is subjected to feedback control such that a read address to read said data from said buffer memory and a write address to write said data into said buffer memory satisfy:

(write address - read address) = a maximum difference.

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--30. (Amended) A recording and playback apparatus having a recording system and a playback system each employing a signal-processing circuit, each of said signal-processing circuits comprising:

a first equalization circuit;

a phase-locked loop circuit for receiving playback data obtained as a result of analog-to-digital conversion of a playback signal by said first equalization circuit; and

a second equalization circuit provided on a downstream side from said phase-locked loop circuit,

wherein each of said first and said second equalization circuits is composed of a transversal filter;

a sampling frequency of said first equalization circuit

is set at a value approximately equal to a channel clock frequency;

a subsequent transfer characteristic of said first equalization circuit is made equal to a product of a present transfer characteristic of said first equalization circuit and a present transfer characteristic of said second equalization circuit; and

a subsequent transfer characteristic of said second equalization circuit is flattened.

93 --31. (Amended) A recording and playback apparatus including a recording system and a playback system each employing a signal-processing circuit, each of said signal-processing circuits comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal;

a digital phase-locked loop circuit for receiving said digital signal from said analog-to-digital converter;

an equalization circuit composed of a digital transversal filter, said equalization circuit being provided between said analog-to-digital converter and said phase-locked loop circuit; and

an interpolation circuit for interpolating separate pieces of sampling data with a period approximately equal to a channel clock period, said interpolation circuit being provided between said equalization circuit and said digital phase-locked loop circuit,